WHAT IS CLAIMED IS:

1. A semiconductor device comprising,

a first semiconductor layer of a first conductivity type,

a second semiconductor layer of the first conductivity type formed in an upper surface of the first semiconductor layer, resistance of the second semiconductor layer being higher than that of the first semiconductor layer,

a base layer of a second conductivity type formed on the second semiconductor layer,

gate electrodes deposited in a plurality of first trenches, a gate insulation film being disposed between inner walls and the gate electrodes, each of the first trenches having a band-shaped planar pattern and extending from top of the base layer down to the upper surface of the second semiconductor layer,

bridge electrodes filling a plurality of second trenches and surrounded by an insulation film deposited over walls of the trenches, the second trenches extending from the top of the base layer down to the upper surface of the second semiconductor layer and connecting adjacent ones of the first trenches in communication with one another so that each of the bridge electrodes electrically connects adjacent ones of the gate electrodes,

an impurity diffused region of the second conductivity type formed in the second semiconductor layer adapted to surround the second trenches existing in the second semiconductor layer,

a source region of the first conductivity type formed in a surface area of the base layer alongside extensions of the gate electrodes,

a source electrode formed on the surface of the source region, and

a drain electrode formed on a back surface of the first semiconductor layer.

2. A semiconductor device according to claim 1, wherein the bridge electrodes are disposed at a predetermined pitch along an extension of the gate electrodes.

3. A semiconductor device according to claim 1, wherein the impurity diffused region of the second conductivity type is formed in the base layer along side walls of the second trenches to reduce carriers induced in the vicinity of the opposite sides of the bridge electrodes upon turning the device on.

4. A semiconductor device according to claim 3, wherein the bridge electrodes are disposed at a predetermined pitch along an extension of the gate electrodes.

5. A semiconductor device comprising,

a first semiconductor layer of a first conductivity type,

a second semiconductor layer of the first conductivity type formed on an upper surface of the first semiconductor layer, resistance of the second semiconductor layer being higher than that of the first semiconductor layer,

a base layer of a second conductivity type formed on the second semiconductor layer,

gate electrodes deposited in a plurality of first trenches, a gate insulation film being disposed between inner walls and the gate electrodes, each of the first trenches having a band-shaped planar pattern and extending from top of the base layer down to the upper surface of the second semiconductor layer,

bridge electrodes filling a plurality of second trenches and surrounded by an insulation film deposited

over walls of the trenches, the second trenches extending from the top of the base layer and being smaller in depth than the base layer, each of the second trenches connecting adjacent ones of the first trenches in communication with one another so that each of the bridge electrodes electrically connects adjacent ones of the gate electrodes,

a source region of the first conductivity type formed in a surface area of the base layer alongside extensions of the gate electrodes,

a source electrode formed on the source region,

an impurity diffused region of the first conductivity type formed around lower portions of the first trenches in the base layer and being contiguous to the second semiconductor layer so as to provide a channel conducting to the source region, and

a drain electrode provided on a back surface of the first semiconductor layer.

6. A semiconductor device according to claim 5, wherein the bridge electrodes are disposed at a predetermined pitch along an extension of the gate electrodes.

7. A semiconductor device according to claim 5, further comprising an impurity diffused region of the second conductivity type formed in the base layer along side walls of the second trenches to reduce carriers induced in the vicinity of the opposite sides of the bridge electrodes upon turning the device on.

8. A semiconductor device according to claim 7, wherein the bridge electrodes are disposed at a predetermined pitch along an extension of the gate electrodes.

9. A semiconductor device comprising,

a first semiconductor layer of a first conductivity

type,

a second semiconductor layer of the first conductivity type formed in an upper principal surface of the first semiconductor layer, the second semiconductor layer being higher in resistance than the first semiconductor layer,

a base layer of a second conductivity type formed in an upper principal surface of the second semiconductor layer,

gate electrodes deposited in a plurality of first trenches, a gate insulation film being disposed between inner walls and the gate electrodes, each of the first trenches having a band-shaped planar pattern and extending from top of the base layer down to the upper surface of the second semiconductor layer,

bridge electrodes filling a plurality of second trenches and surrounded by an insulation film deposited over walls of the trenches, the second trenches extending from the top of the base layer and being smaller in depth than the base layer, each of the second trenches connecting adjacent ones of the first trenches in communication with one another so that each of the bridge electrodes electrically connects adjacent ones of the gate electrodes,

a source region of the first conductivity type formed on a surface area of the base layer alongside extensions of the gate electrodes,

a source electrode formed on the source region, and

a drain electrode provided on a back surface of the first semiconductor layer.

10. A semiconductor device according to claim 9, wherein the bridge electrodes are disposed at a predetermined pitch along an extension of the gate electrodes.